SiC Megawatt Technology Annual Briefing

October 17, 2000

NORTHROP GRUMMAN

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Agenda

- Overview
- Process Development
  - JTE
  - Devices
    - Diodes
    - GTOs
    - JFETs
- Package Development
  - SPCO Package Approach
  - K Technology TPG encapsulated material
- CHPS applications

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Megawatt Program Objectives

- Develop SiC Power GTO, JFETs and pn junction diodes with capability up to 5000V/1000A for use in Utility Power Systems
- Achieve intermediate goals of 1kV/5A devices to support Combat Hybrid Power Systems Flywheel Inverter construction
- Initiate the development of a packaging approach for a 5kV/200A package

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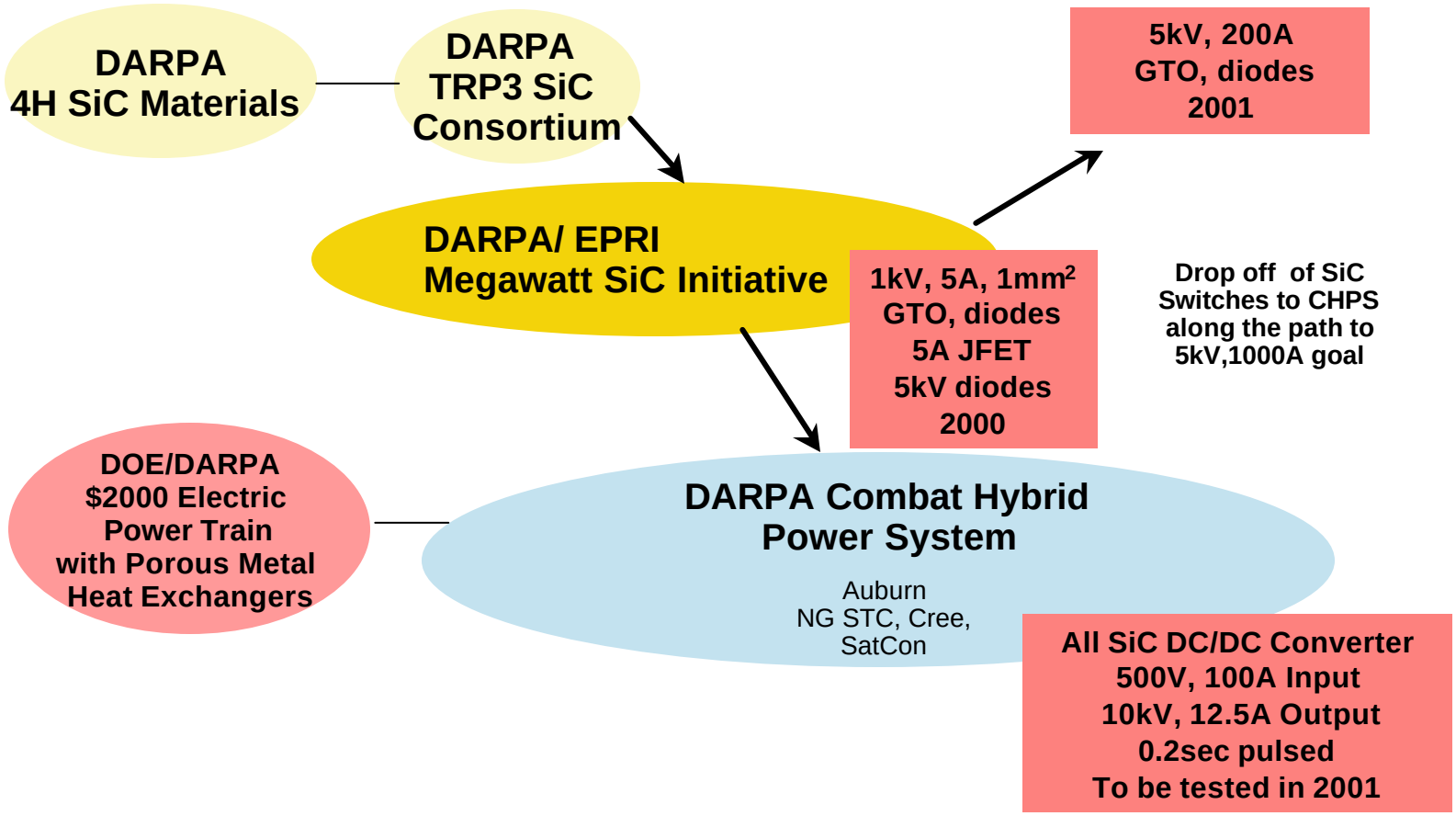
SiC Evolution



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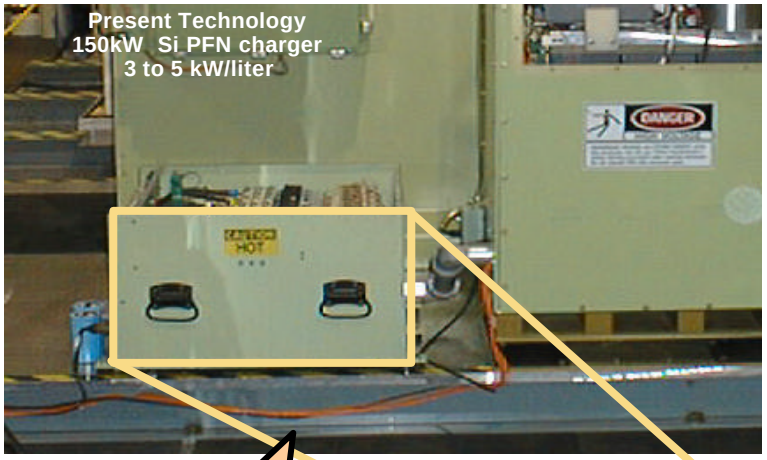
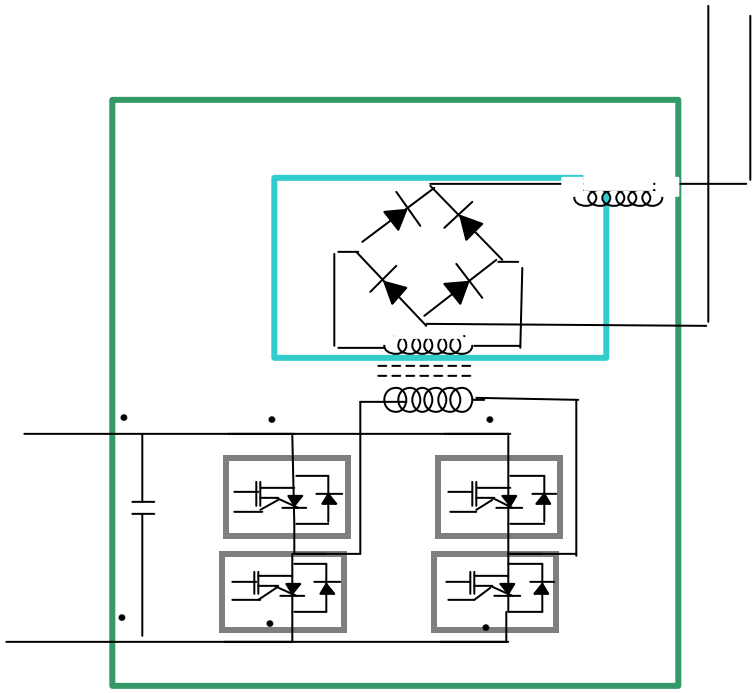
SiC DC/DC Converter demonstrates merits of higher frequency and temperature



50 kW/liter
10 X Size
Reduction

Technology
Impact



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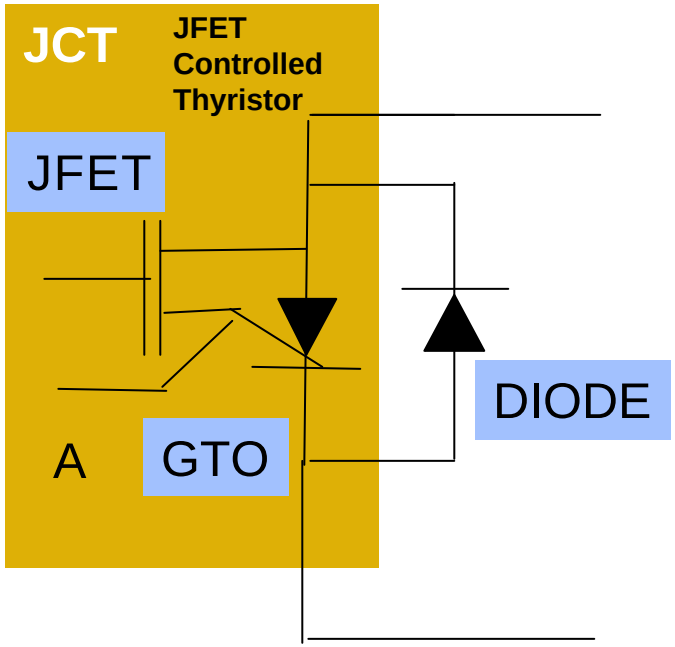
Building blocks for high power converters and Utility power handling applications



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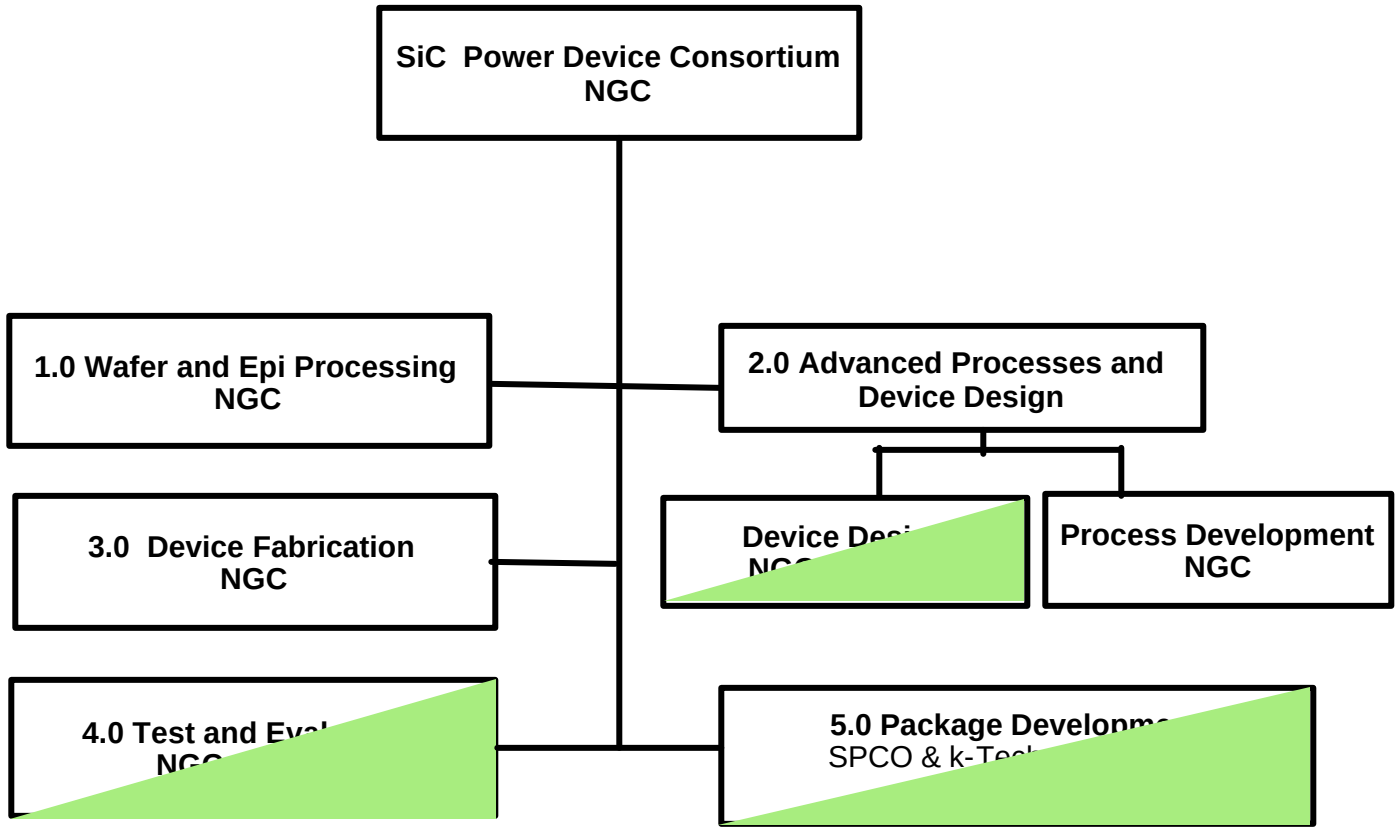
Program Organization



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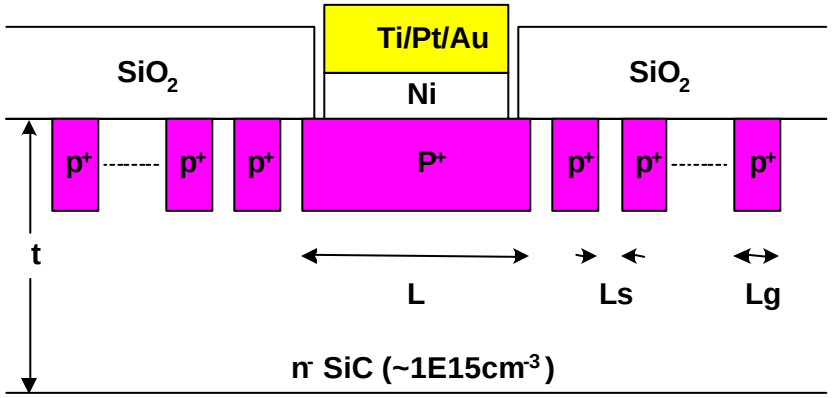
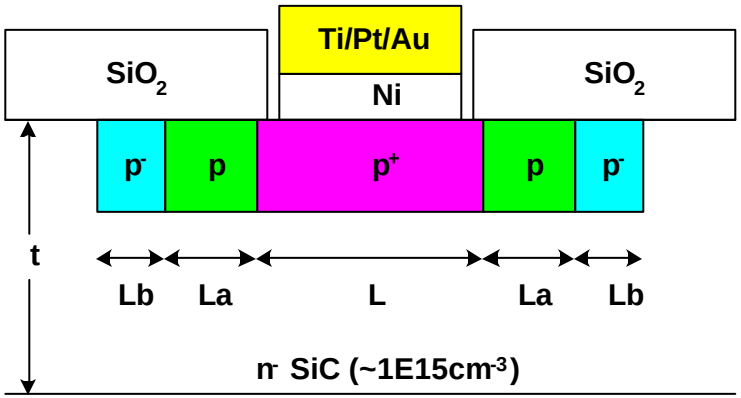
Edge Termination

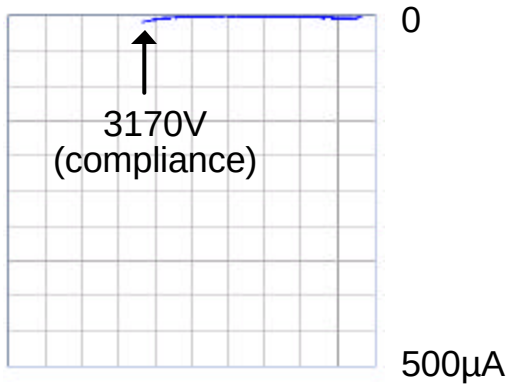
GR (15 rings max)



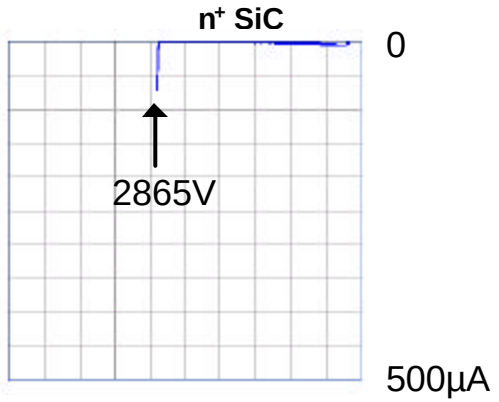
JTE (2 zone)



1mm GR Diode



1mm JTE Diode



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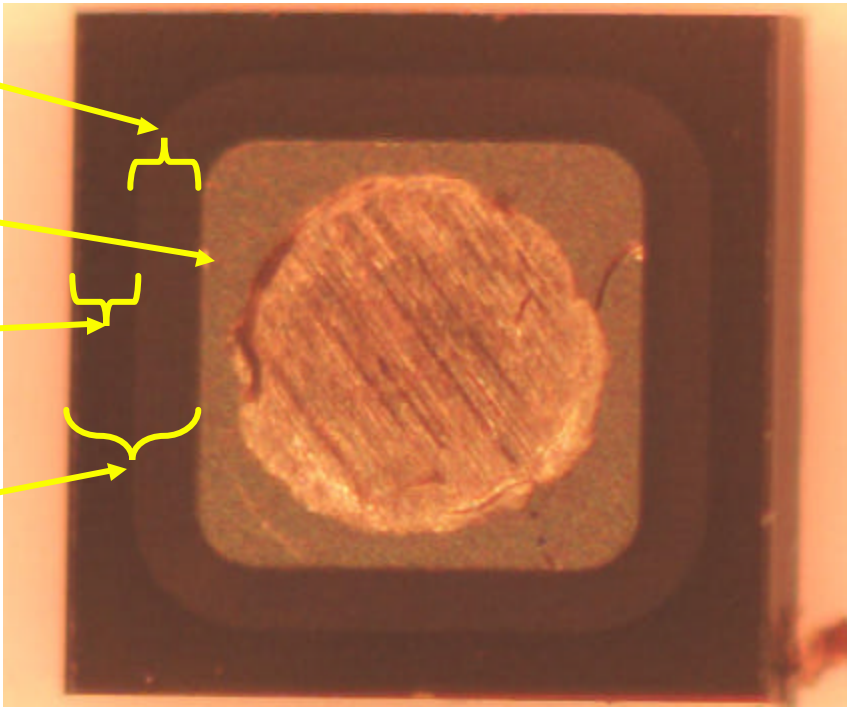
High Voltage Diode Edge Termination



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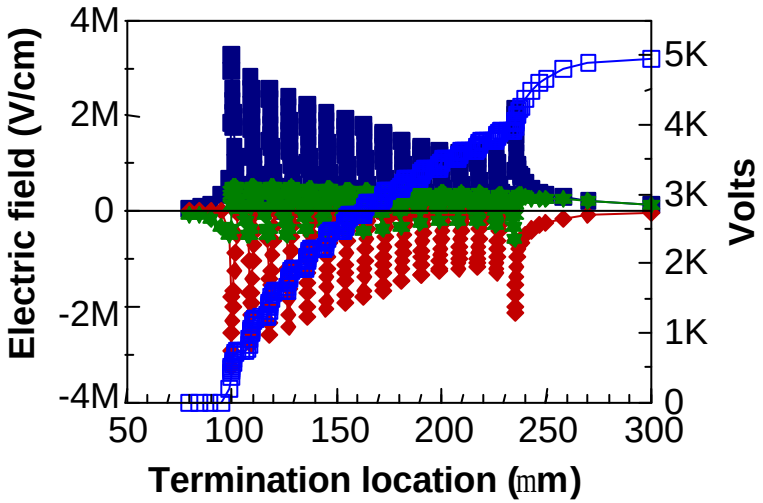
Multizone JTE reduces Surface fields by Order of Magnitude

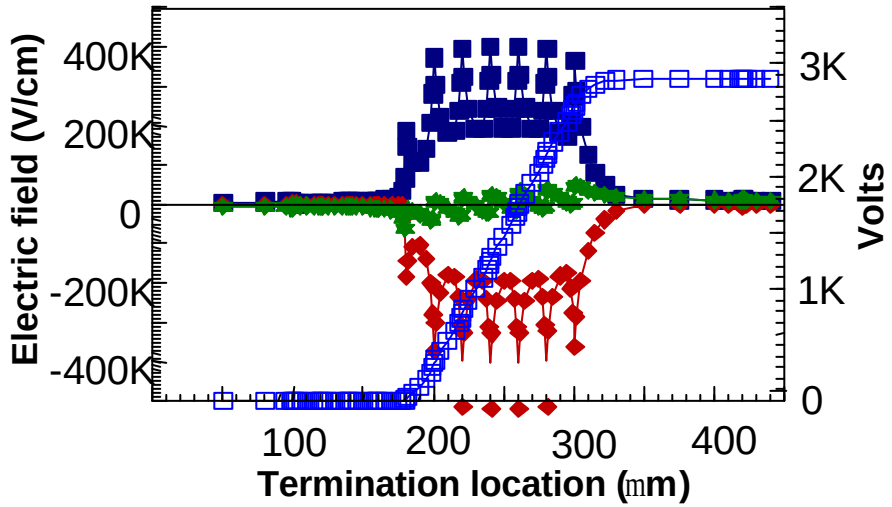
Surface field and voltage for 15 field rings

Peak surface Field=4E6 V/cm



Surface field and voltage for a 10 zone JTE

Peak surface Field = 4E5 V/cm



□ Voltage ◆ Surface E Field ★ Normal E Field ■ E Field

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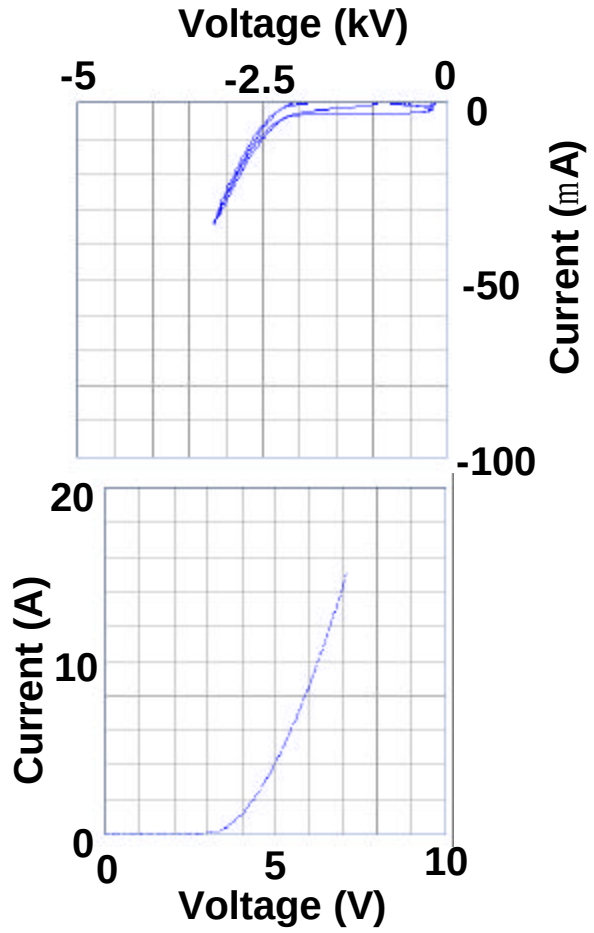
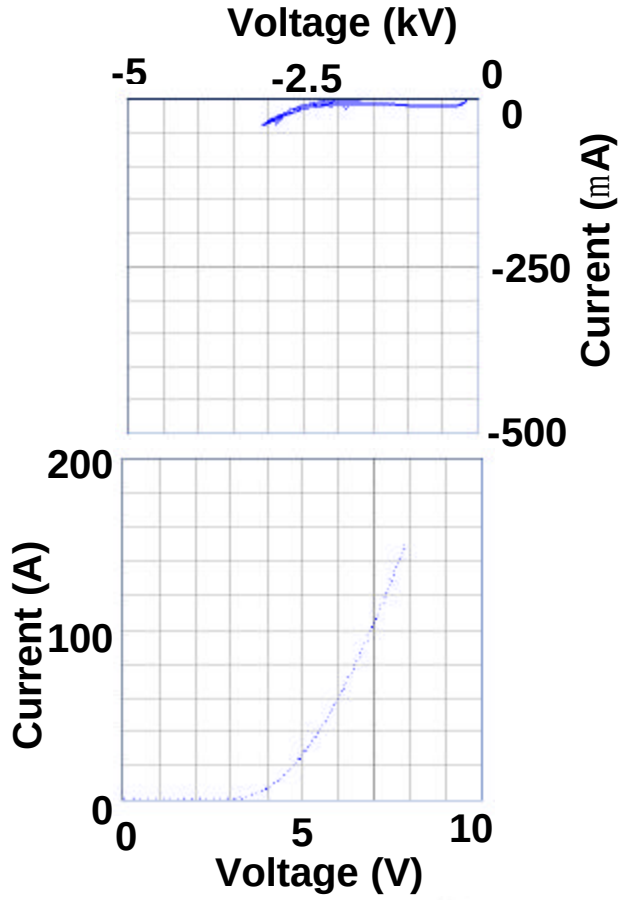
Single Diode achieves >3KV and >10A
Assembly achieves >3KV & >100A





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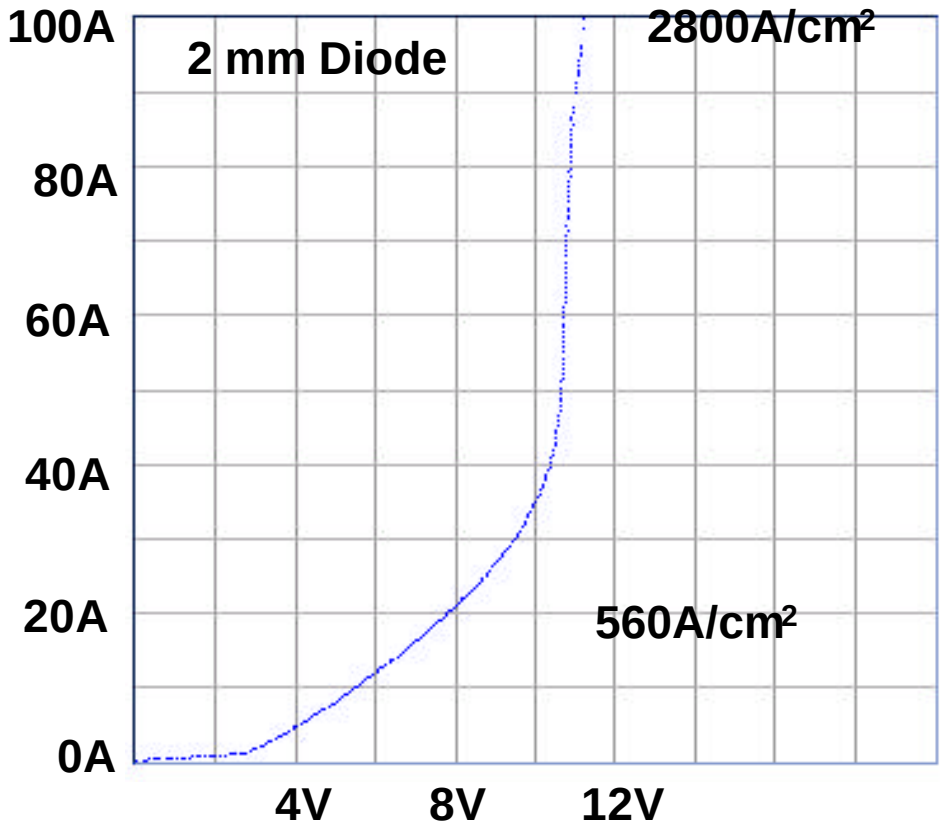
SiC is incredibly rugged



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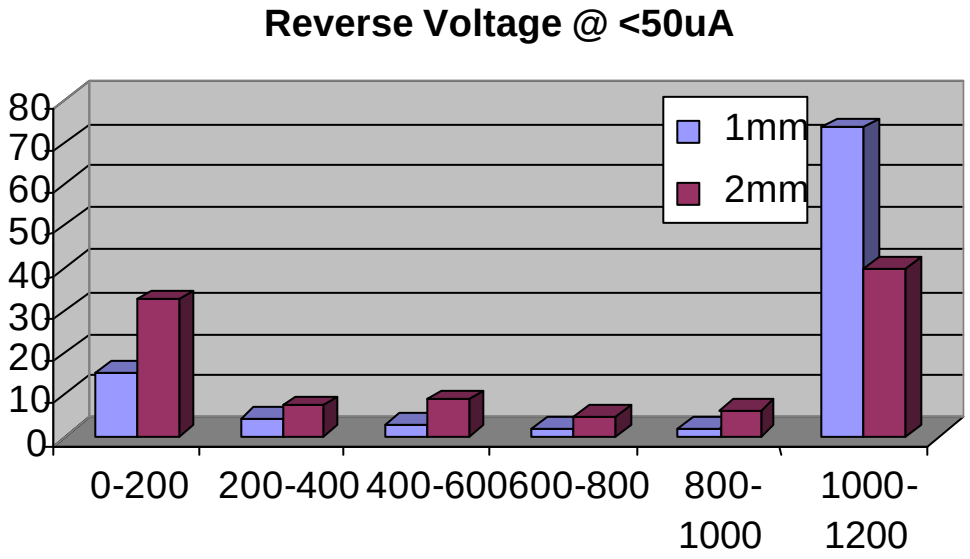
Diodes show >70% yield



-Strong dependence on epi quality
-Reasonable (40%) yields even at 2 mm

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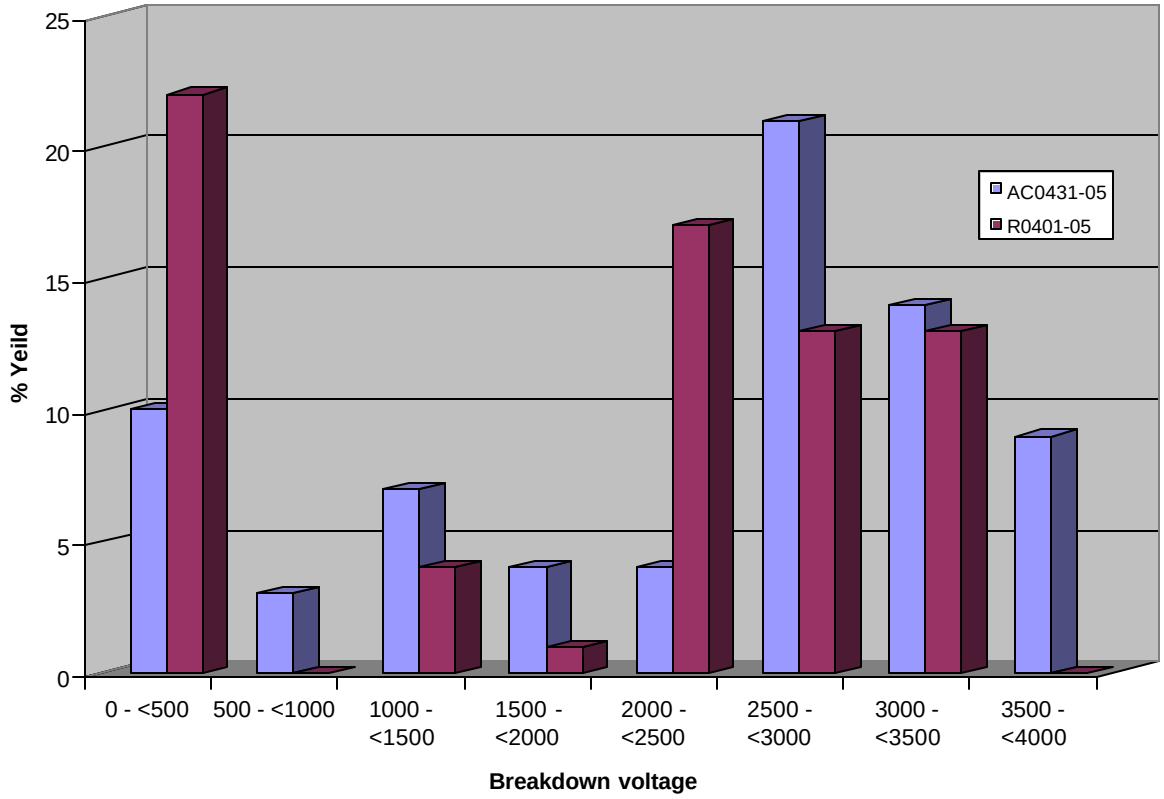
High Voltage Diode Yield



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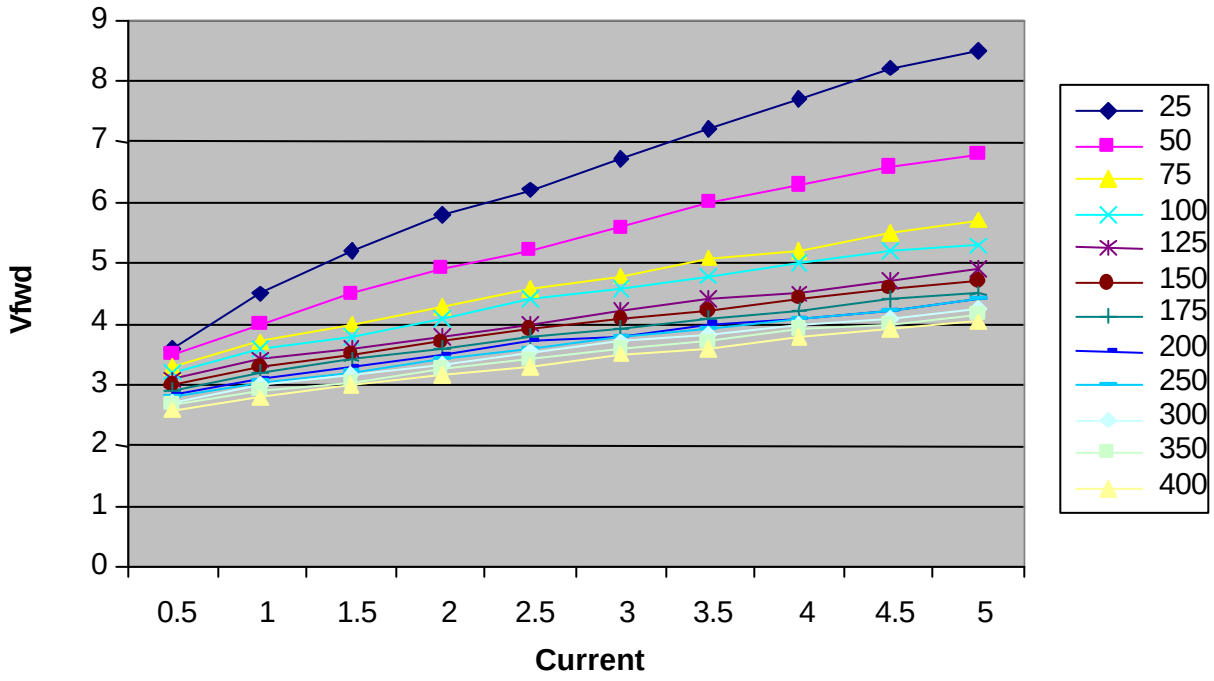
Forward drop decreases with temperature

Fwd V vs. I as a function of Temperature



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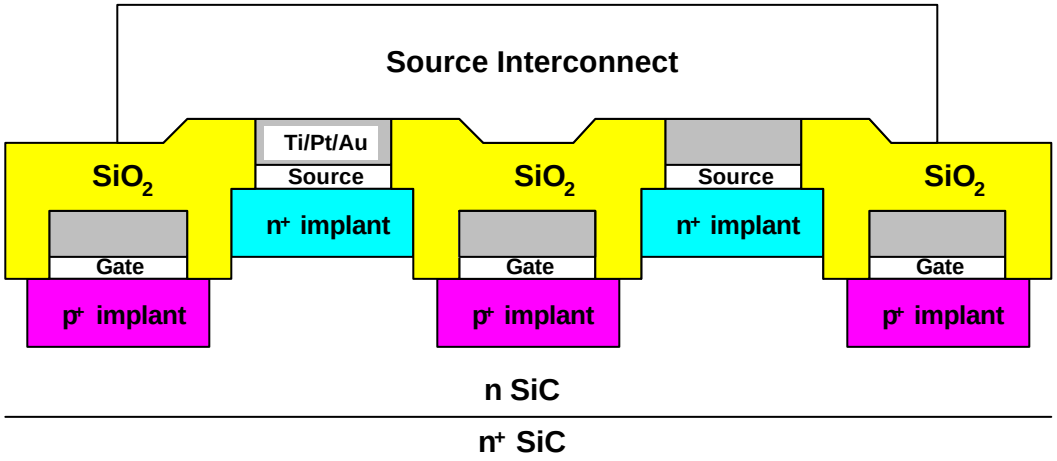
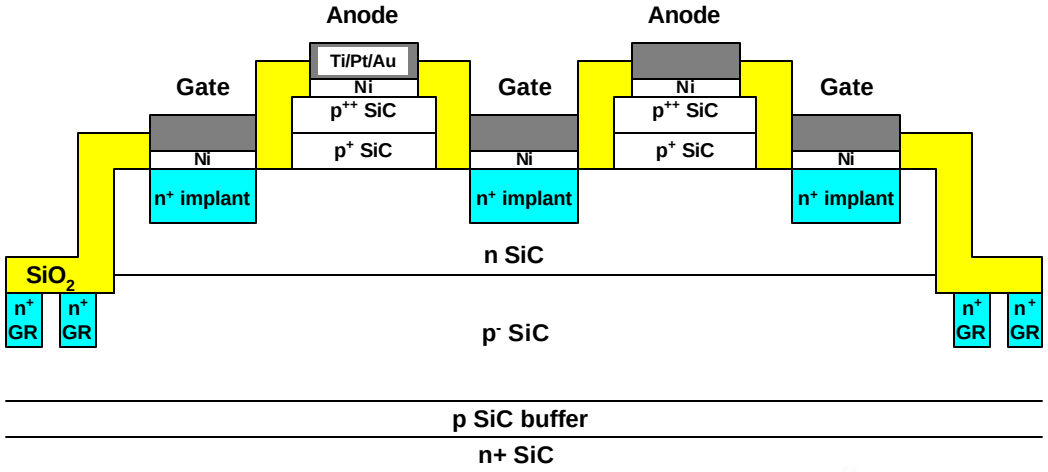
JFET & GTO



JFET

GTO



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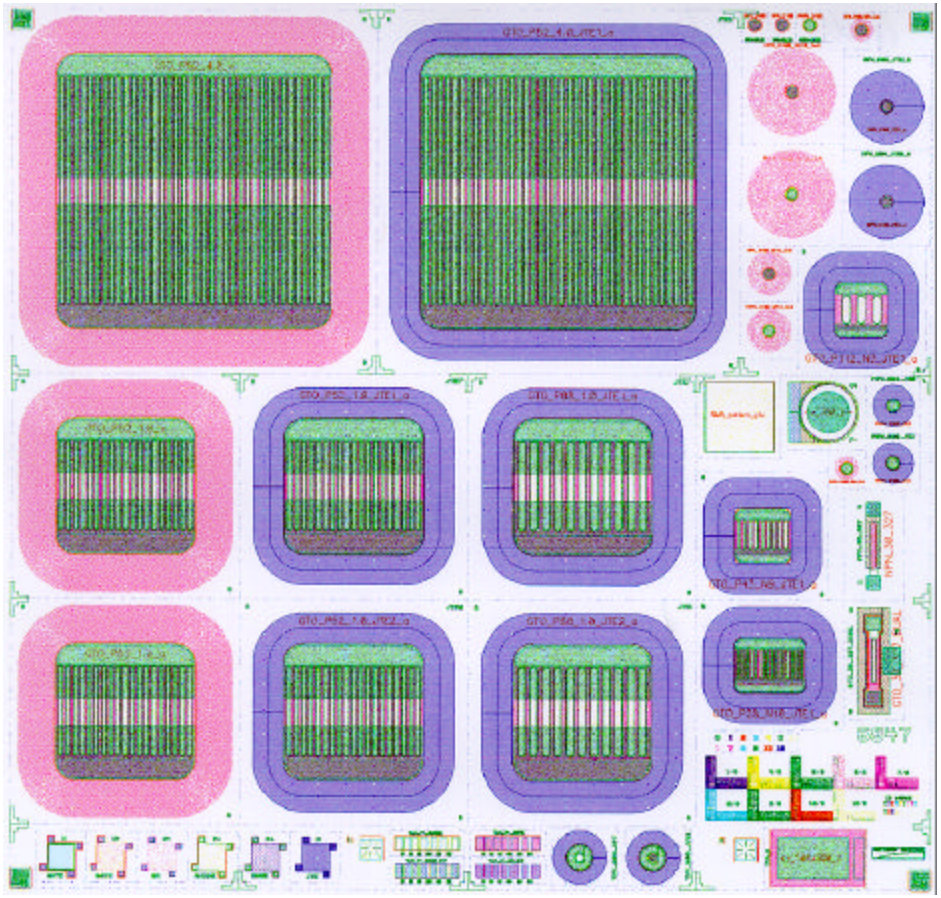
GTO Device Development



- GTO anode finger designs:

- GTO edge terminations:
  20 GR
  20 zone JTE

- pnp and npn BJT test structures

- pnpn and npn test diodes with GR and JTE edge terminations

- PCMs for evaluation of:
  Electrical properties of top 4 layers
  Ohmic contacts
  Electrical activation of implants

- Area for SIMS analysis

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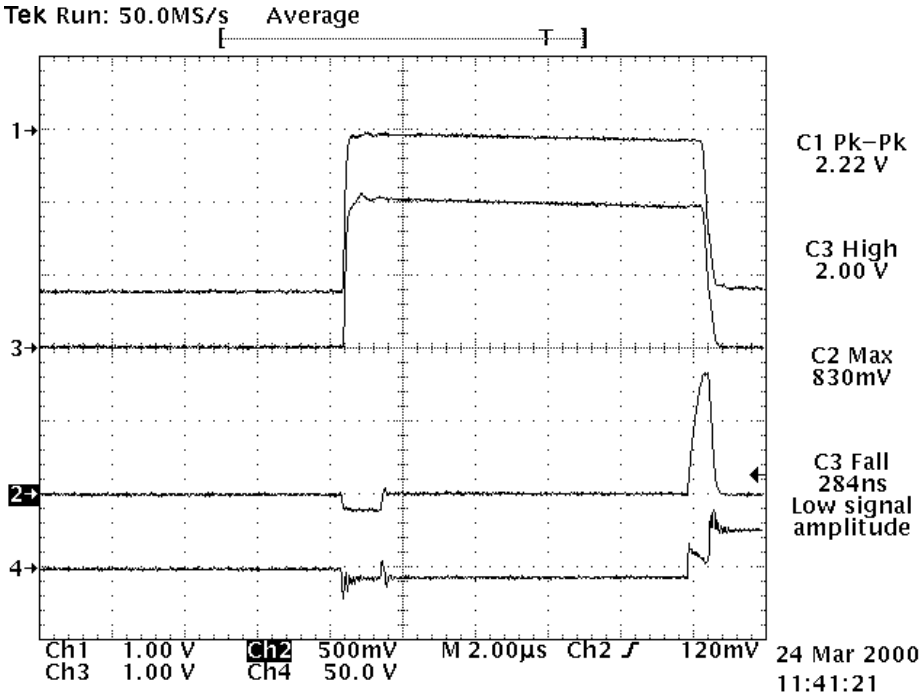
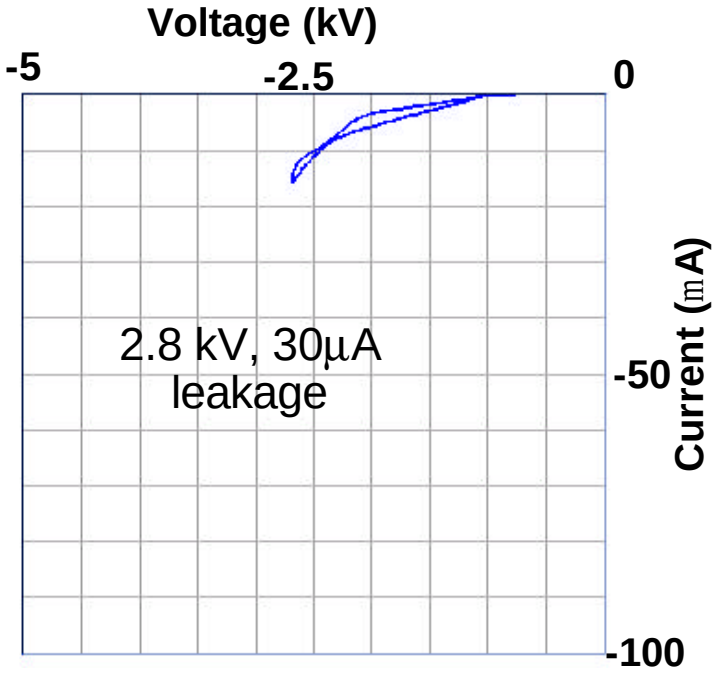
1mm GTO achieves 20A cell
2mm GTO achieves 2.8kV





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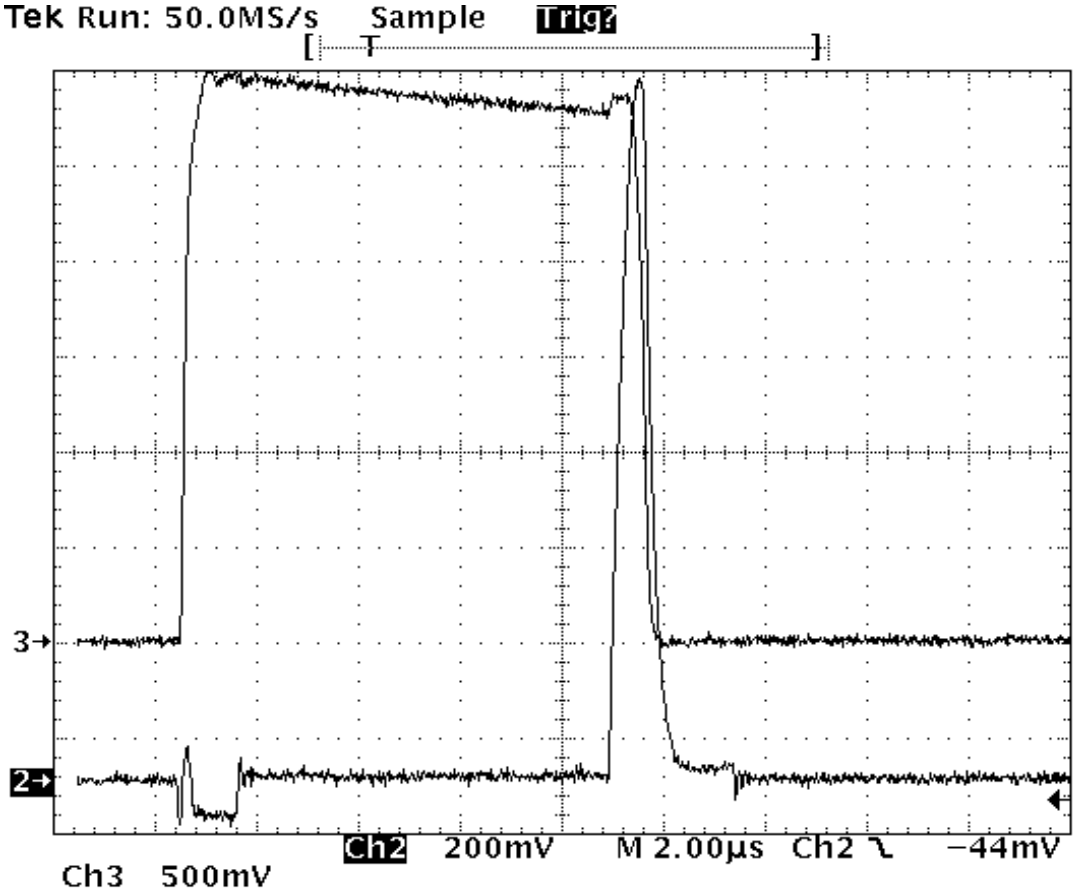
30A assembly



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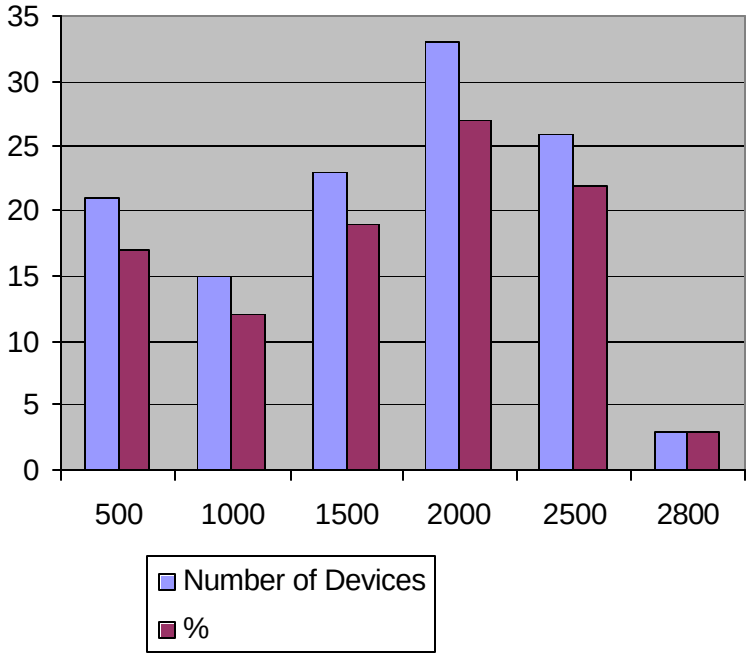
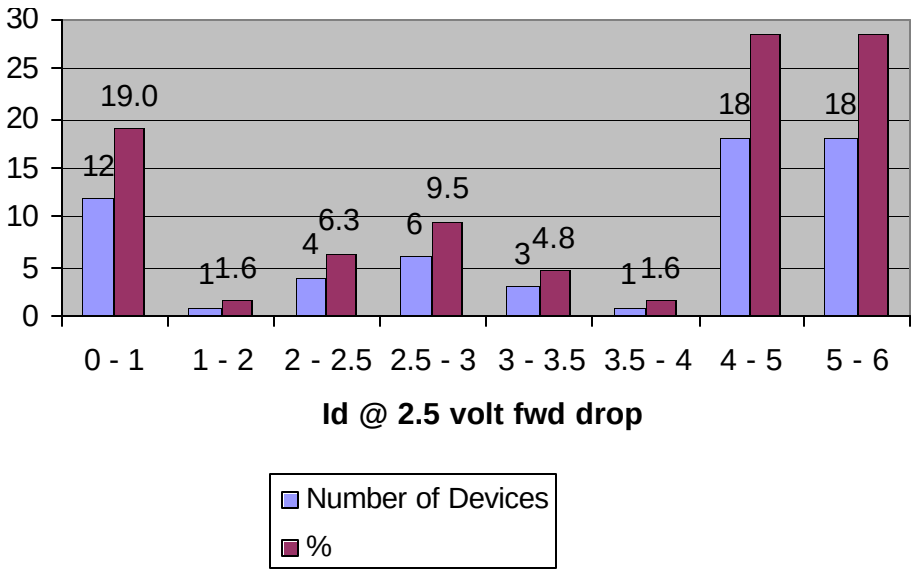
GTO Yields ~ 25%@ 2 kV
JFET Yields >50% @ 4A

30 micron GTO



JFET



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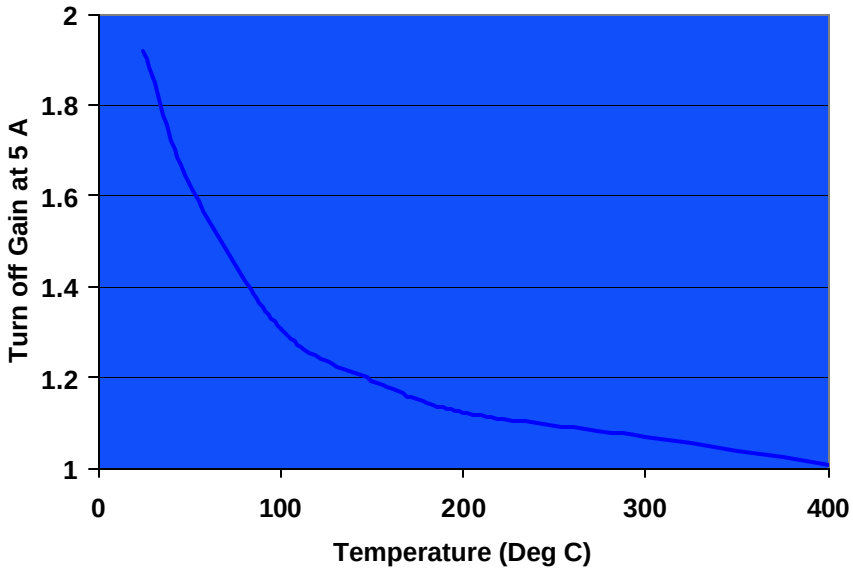
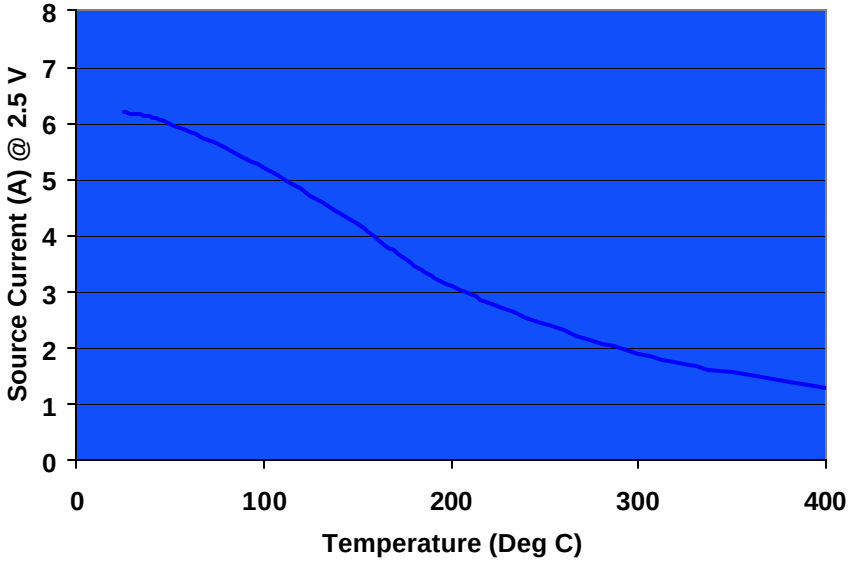
Turn off Characteristics for JCT

GTO Turn off Gain



JFET Current



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Device Summary

- Phase I and Phase 2 device goals exceeded

	Phase 1	Phase 2
•	Diode: 2A cells,30A, 2kV	10 A cell, 100A, 3kV
•	GTO: 2A cells, 30A, 2kV	10A cell, 30A, 2.8 kV
•	JFET: 1A cells, 5A	2.5A cell, 25A

- Demonstrated 30A JCT
- Yields for 1mm above 50%,
- Yields for 2mm are encouraging- >30%

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SPCO is packaging JCT

Design Specifications

- Current: 200 Amperes
- Voltage: 3kV
- Temperature range: RT - 250C
- Power density up to 1250 watts/cm^2
- Device Specs:
  - RT:
    - GTO - 2mm x 2mm/ 20Amp @5 Volts
    - JFET - 1mm x 1mm/ 3Amps @ 2 Volts
  - 250C
    - GTO - > 20Amp @5 Volts
    - JFET - 1.0Amps @ 2 Volts

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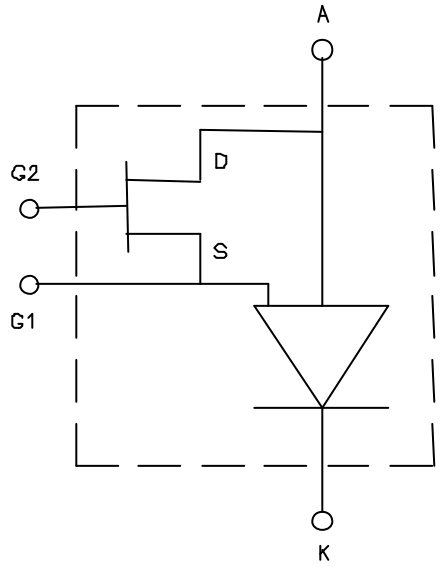
JCT Critical Design Issues

- **High GTO power density:**
  20A/5V/ Area= .04 cm²/50% Duty
  ➡ 1250 Watts/cm²
- **High temperature**
- **Inductance in gate ckt.**
- **Resistance in gate ckt.**
- **Height variations from device to device can result in large mechanical stress when paralleled.**
- **High E-field on top side of GTO cell (3kV across 220 μm gap)**



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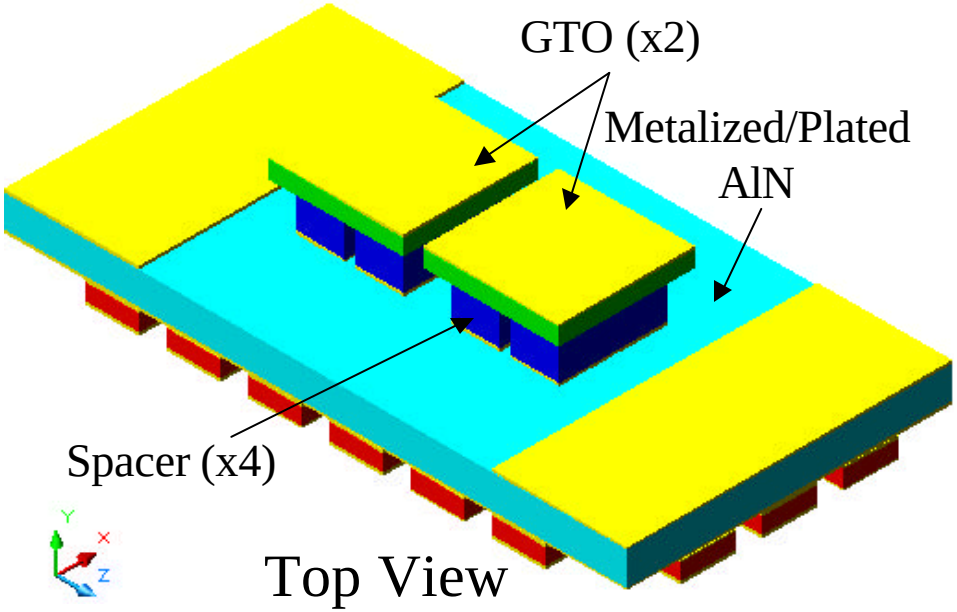
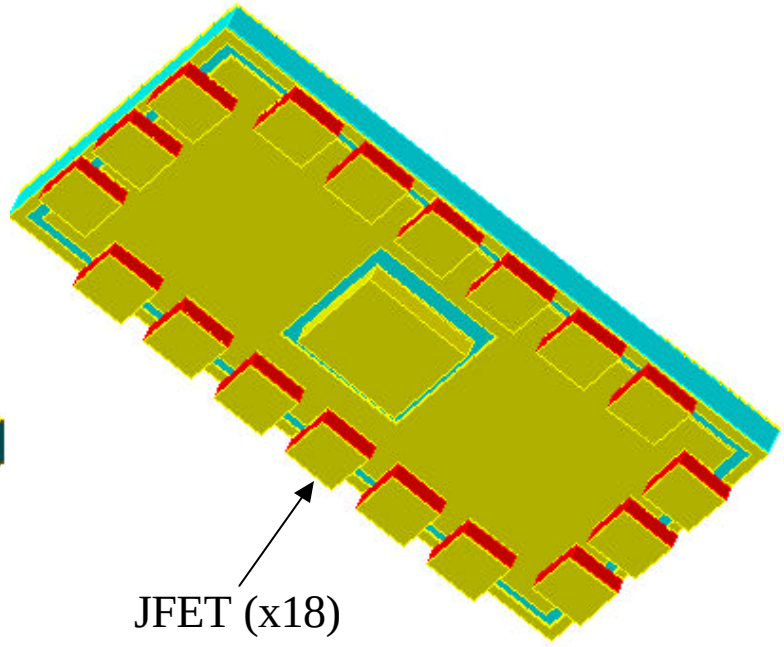
40 Amp JCT Module



Top View



Bottom View

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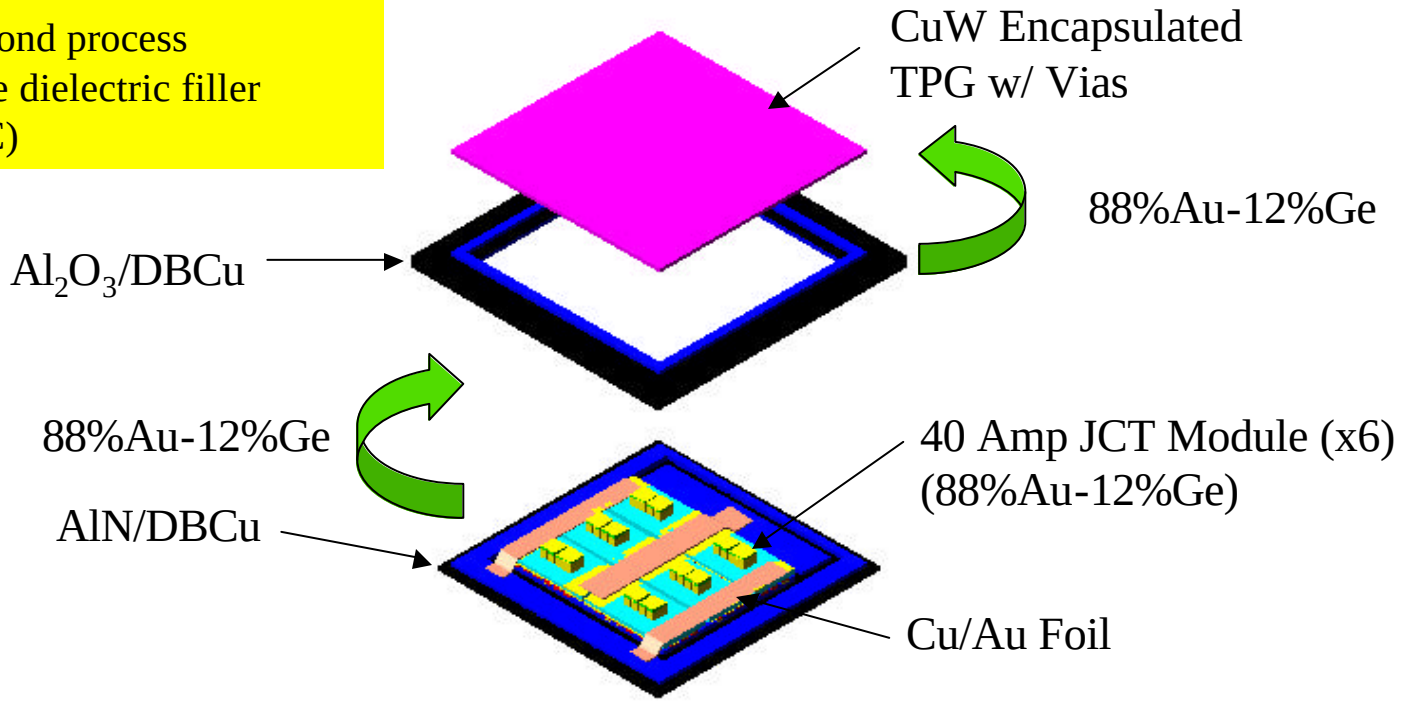
200 Amp Package Design

- Dimension: 1.440”(36mm) x 1.440”(36mm) x 0.200”(5mm)
- 12 GTOs
- 108 JFETs
- 3 stage Au-Ge bond process
- Zerconia Silicate dielectric filler (225v/mil, >500C)



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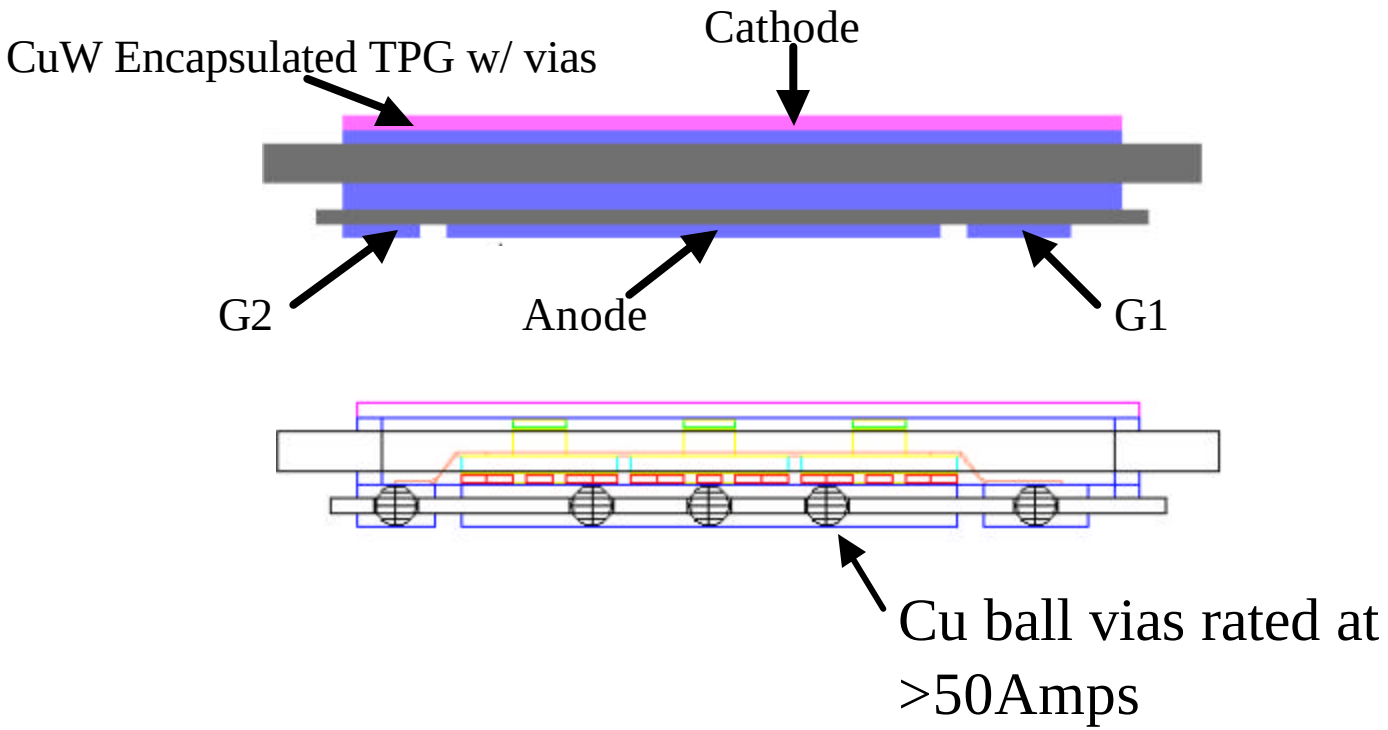
200 Amp JCT Package
(Continued)



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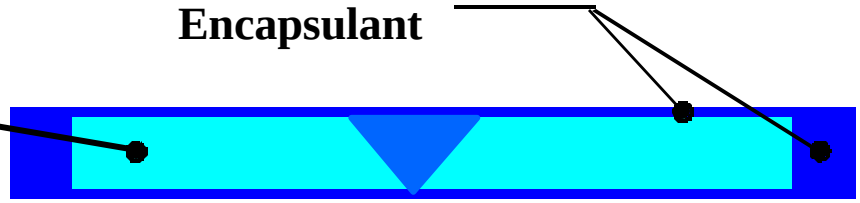
TPG enhances thermal conduction

Thermal Pyrolytic Graphite (TPG)
Kxx=Kyy = 1700 W/mK
Kzz=10 W/mK



- **Material Concept**
  - **The TPG Insert Provides a High Thermal Conduction Path**
  - **The Encapsulation Material Provides Tailorable CTE Mounting Surface**
  - **There Is Negligible In-plane Structural Coupling Between the TPG and Encapsulant**

TPG Properties

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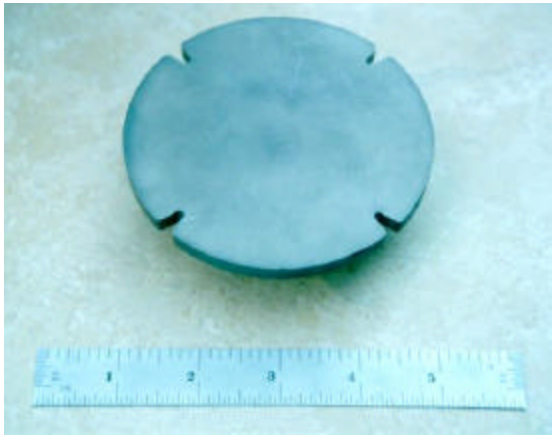
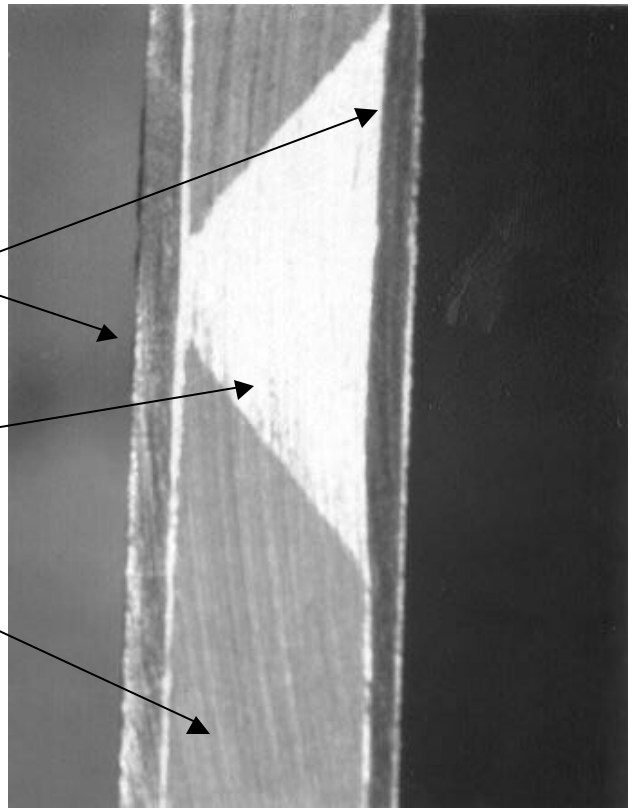
TPG Encapsulation Demonstration

TPG Insert

AlSiC/TPG Heat Spreader





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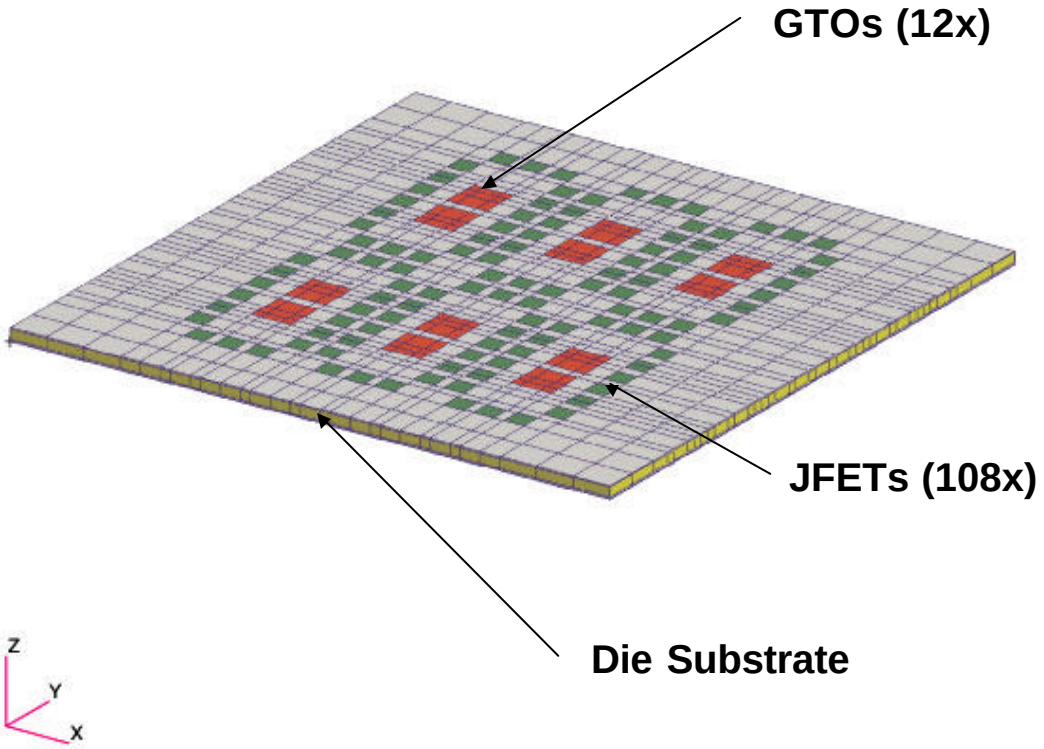
200 Amp Package Thermal Analysis

- Finite Element Model
  - **ABAQUS Finite Element Code**
  - **3D Heat Transfer Element**
  - **4800 Nodes**
  - **3393 Elements**
  - **Processed on HP C3000 Platform**



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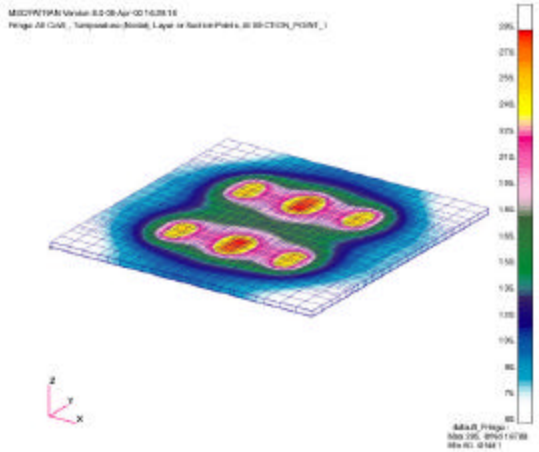
Thermal Analysis

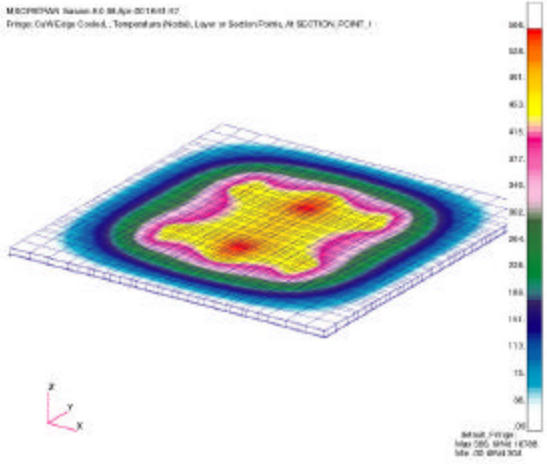
Case 1

- Back Surface Convection
- Material - CuW
- Thickness - 0.6mm
- Maximum Temperatures
  - 285°C at GTO
  - 235°C at JFET



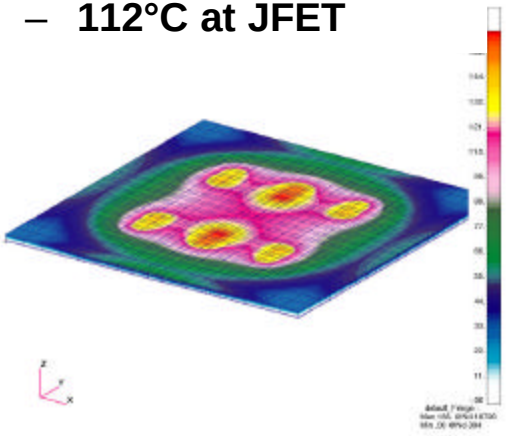
Case 2

- Circumferential Cooling
- Material - CuW
- Thickness - 0.6mm
- Maximum Temperature
  - 566°C at GTO
  - 515°C at JFET



Case 3

- Circumferential Cooling
- Material - CuW Encapsulated TPG
- Thickness - 0.6mm
- Maximum Temperature
  - 169°C at GTO
  - 112°C at JFET



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Summary

- Megawatt demonstrates enhanced thermal and electrical properties of SiC
- As substrates are improved larger devices will be feasible
- Single Devices achieve >500W/cm, >20A, >3kV
- Advanced packaging concepts will integrate a 200A package with advanced TPG materials
- CHPS will provide a near term demonstration

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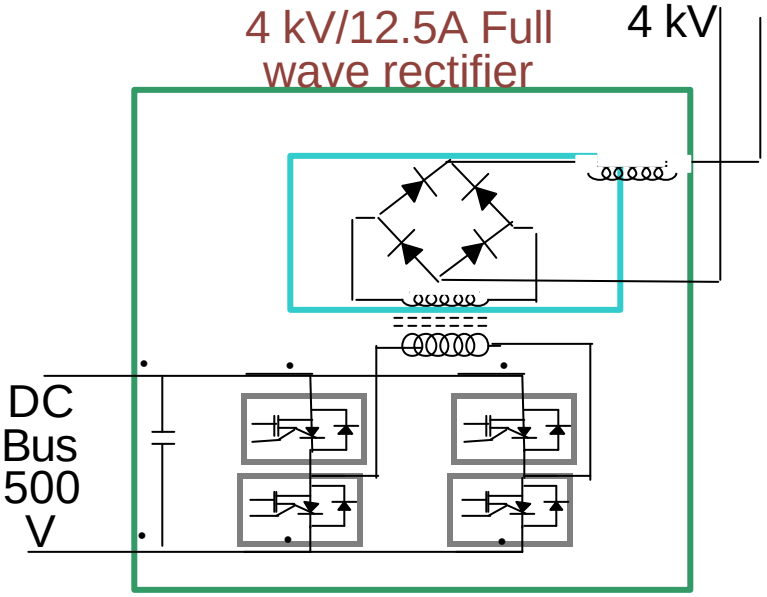
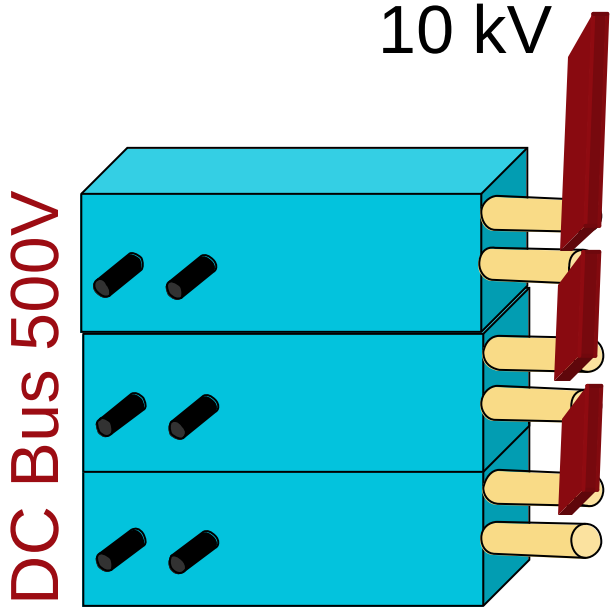
CHPS Air cooled, upgradable modules deliver 0.2 sec pulse at 150 kW



Module holds 500V/100A H Bridge with four 100A sandwiches 400C junction temp. on switches and 250C on rectifier 100 kHz



Three 50 kW modules in series to achieve 10kV and 150kW for 3 modules in series

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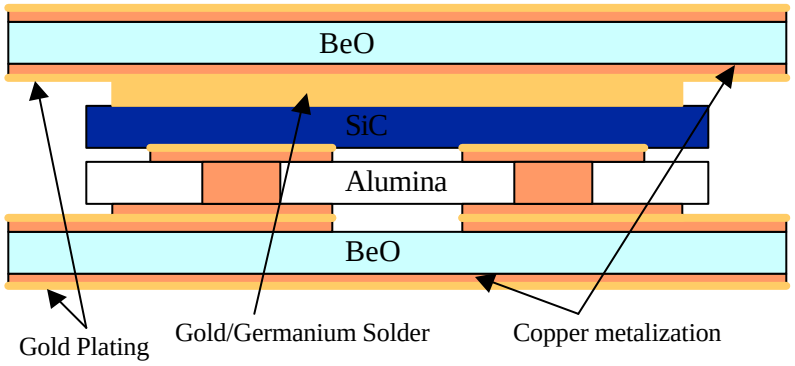
AUBURN ENGINEERING

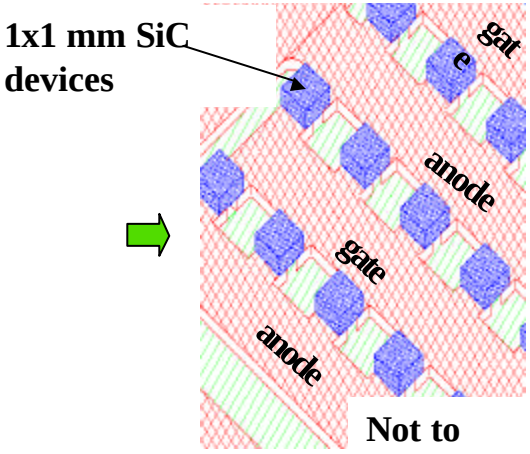
SatCon

CREE

CHPS Combat Hybrid Power Systems

First samples of Substrates using BeO for both Switch and Rectifier received

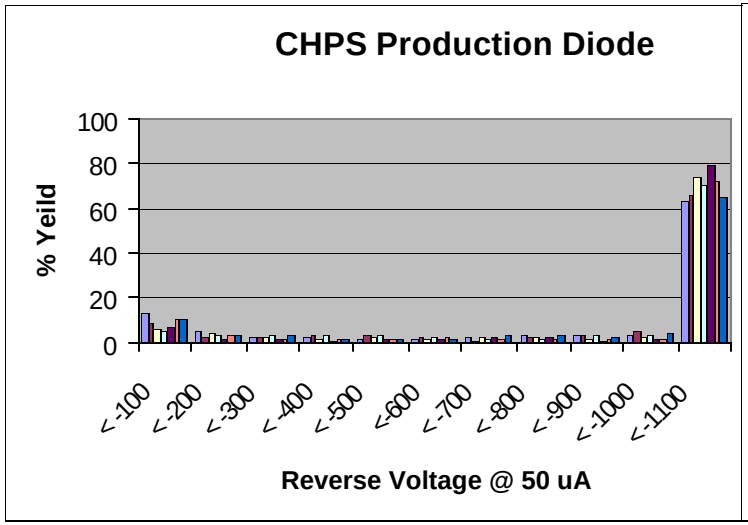




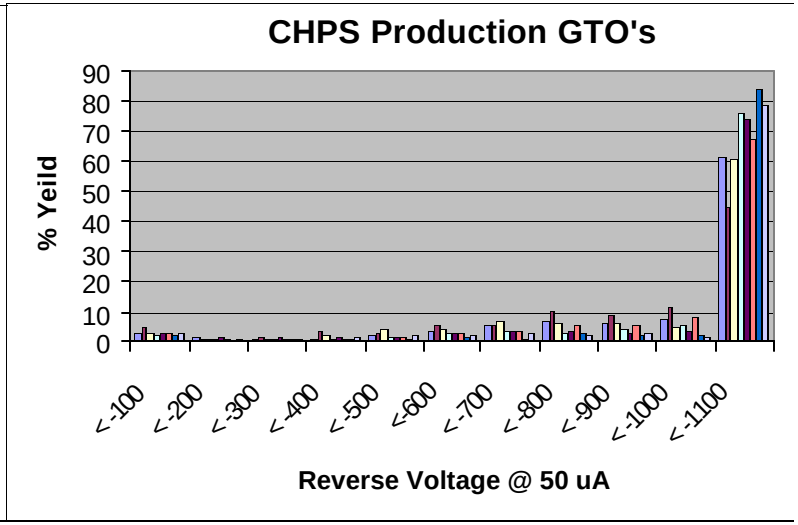
- **We have settled on BeO as the substrate material**
  - AlN process needs more development--- beyond CHPS
  - In addition to better yields, this drove the selection of 1x1mm devices.
- **Sandwich Implementation indicates basic approach works**
  - 100A Switch Design in Progress
  - Alumina Feedthrus production process optimized

Device Yields have been Good

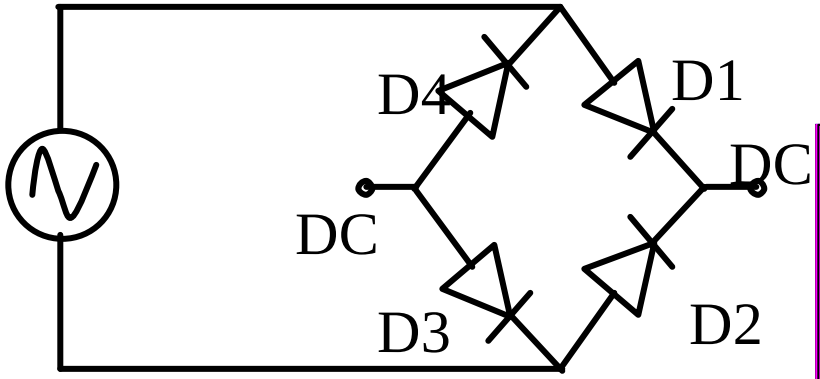
Low Voltage Diode Yield - 70%

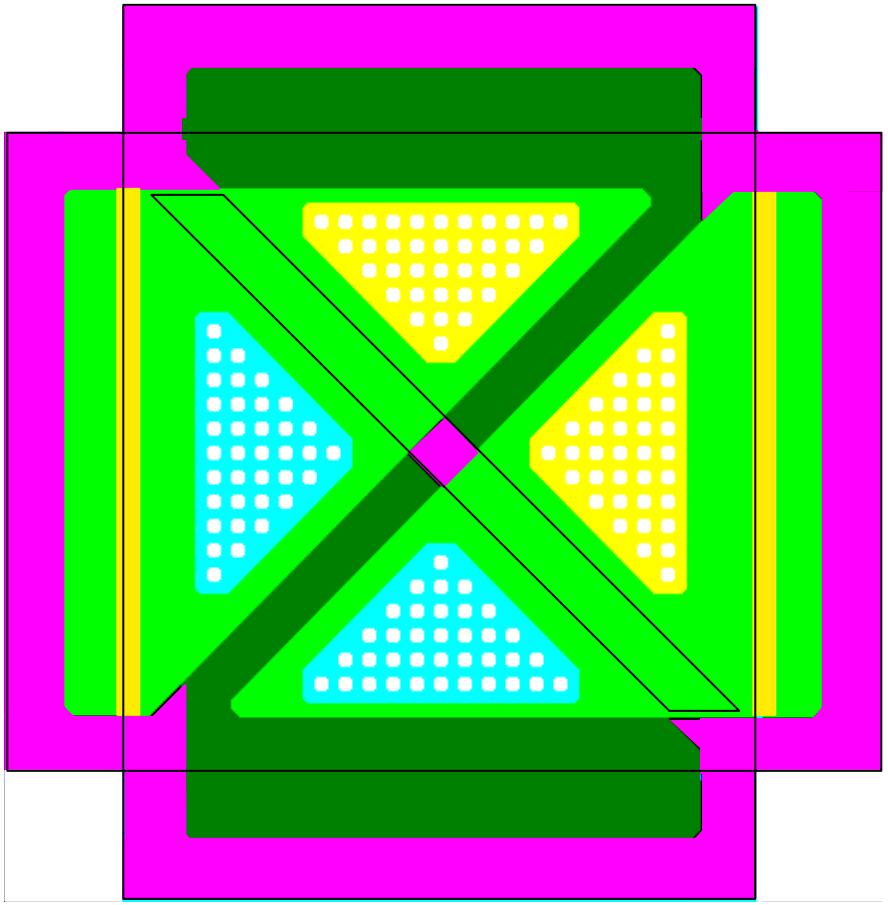


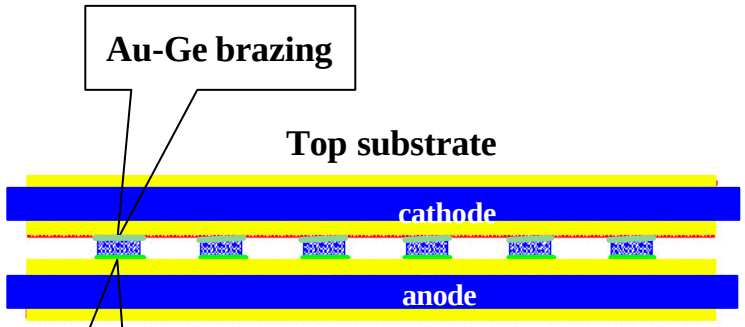
GTO Yield - 53%



Rectifier







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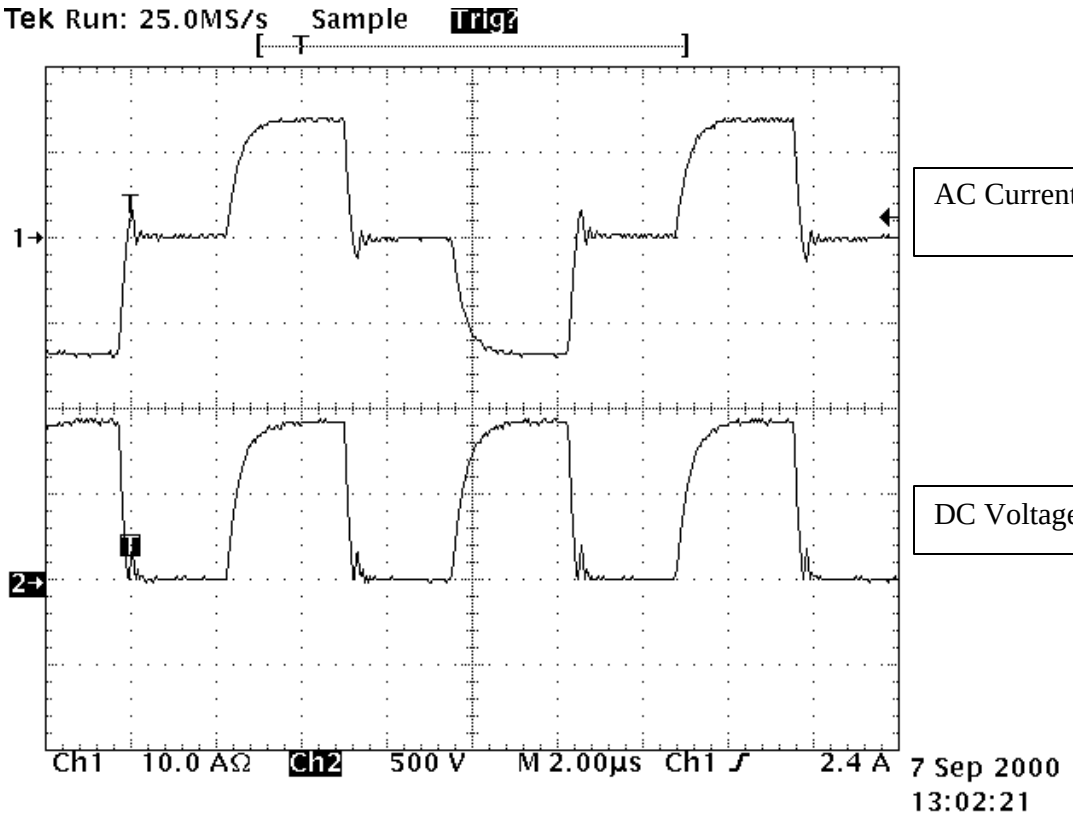
Rectifier - 14A @ 1kV & 100kHz

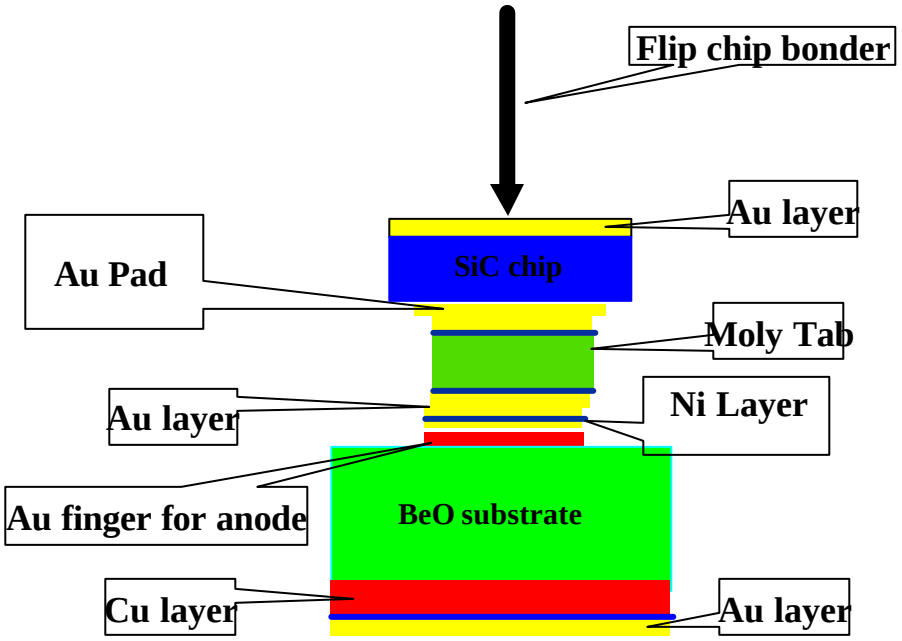


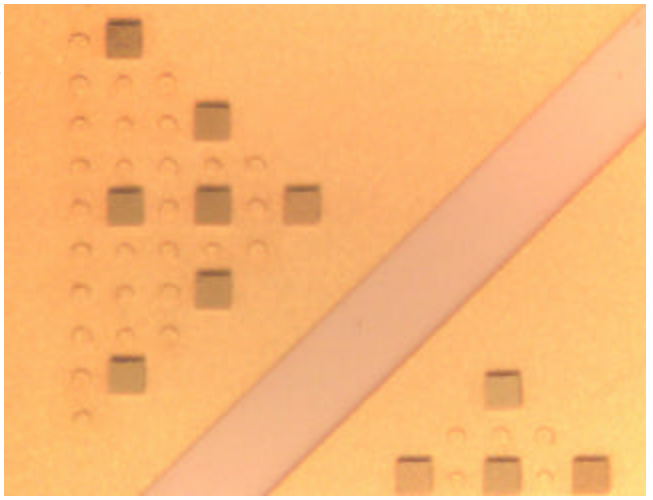
AC Current

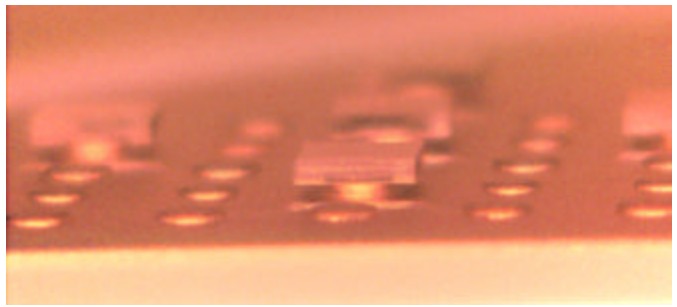
DC Voltage

Thermo-compression Bonding of Die

- Process: 380°C for 120 sec at 3-6 kg in air
- High temperature bond: Au-Au solid diffusion







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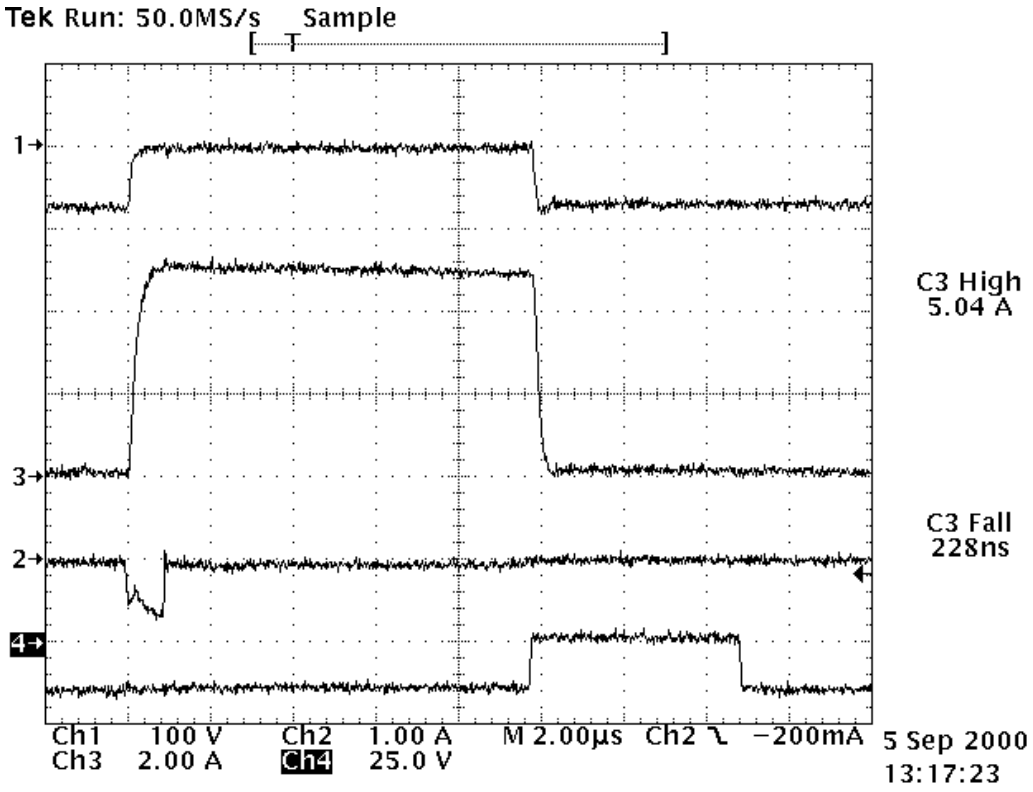
Switch Sandwich

Switch #1 - 5A at 400V



Switch Voltage

Switch Current

GTO Gate Current

JFET Gate Voltage